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| CSE 231 PROJECT REPORT |
| Group 7 Section 1 |
| Fall 2017 |

*Group Members*

*Syeda Natasha Nafreen*

*ID -1520704642*

*Mahbuba Tasmin*

*ID – 1610064042*

*Abidur Rahman Tawsif*

*ID – 1611822642*

*Raisa Taraman Shithi*

*ID -1610190642*

*Submitted to*

*Dr.Arshad M Chowdhury*

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* Project Idea Statement

This project aims to produce a display sequence of a given string “**CSE231-Sec-Team no”** on a single 7 segment display. The display sequence depends on the input and move thereby.

It has two main phases; combinational phase and sequential phase. In combinational phase, the sequence is derived manually where the sequential phase gives the automated sequence one after another after a single input is given.

* Abstract

We have completed the combinational part using 3 bit input where we discarded the repeated sequence (**CSE231- Team no)** of section number since it is already prepared in “231”. From this combinational part, we have designed a sequential phase considering an extra bit for the repeated sequence (5 bits table including input) that will correctly give the output sequence as outlined in the project description.

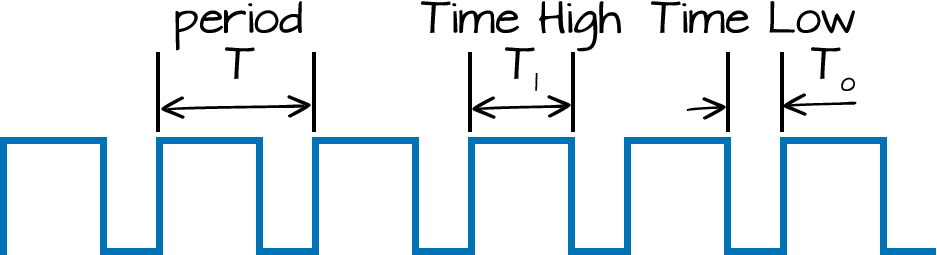
* List of Equipment

|  |  |  |
| --- | --- | --- |
| **Phase name** | **Equipment** | **Quantity** |
| **Combinational Circuit Design** | IC 74238(3:8 Decoder(Active high)) | 1 |
| IC 7432 (2 –input OR) | 2 |
| IC 4075(3-input OR) | 1 |
| **Sequential Circuit Design** | IC 7473( Dual Master JK Flip Flop) | 2 |
| IC 7411 ( 3-input AND) | 2 |
| IC 7408(2- input AND) | 2 |
| IC 7404(Inverter) | 1 |
| IC 7432( 2-input OR) | 1 |
| IC 4075( 3-input OR) | 1 |
| **Timer Circuit** | IC HA555 | 1 |
| Capacitor(100 μF) | 1 |
| Capacitor(10nf) | 1 |
| Resistors(10k) | 2 |
| **Extra utilities** | 7 Segment Display( Common Cathode) | 1 |
| 9V Battery | 1 |
| IC 7805(linear voltage regulator) | 1 |
| Jumper Wires |  |
| Bread Board | 3 |
| Resistor(1k) | 1 |

* Theory

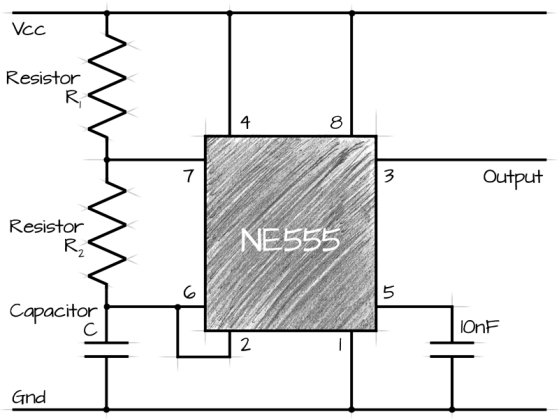
555 Timer IC:

The 555 timer is capable of being used in astable and monostable circuits. In an astable circuit, the output voltage alternates between VCC and 0 volts on a continual basis.



By selecting values for R1, R2 and C we can determine the period/frequency and the duty cycle. Duty cycle is the mathematical parameter that forms a relation between the high output and the low output. Duty Cycle is defined as the ratio of time of HIGH output i.e. the ON time to the total time of a cycle.

The period is the length of time it takes for the on/off cycle to repeat itself, whilst the duty cycle is the percentage of time the output is on. i.e. T1/T. In this type of circuit, the duty cycle can never be 50% or lower.



Here, R1 = 10Ω ,R2 = 10Ω Capacitor = 100μF

* Combinational Phase

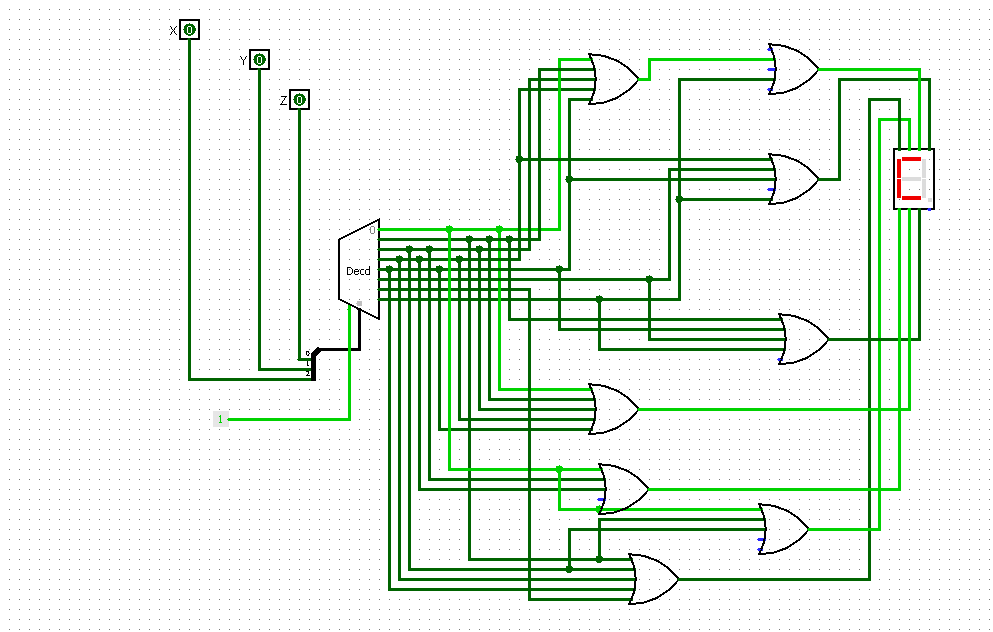
|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| States | Inputs | | | Display decoder pins | | | | | | |
|  | **X** | **Y** | **Z** | **a** | **b** | **c** | **d** | **e** | **f** | **g** |
| **C** | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| **S** | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| **E** | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| **2** | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| **3** | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| **1** | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| **-** | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| **7** | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

Truth Table:

Function Minimization

We have used a 3 to 8 active high decoder , hence we didn’t go through any function minimization process( K-maps) but used the minterms effectively so that the circuit is as minimized as possible.

Circuit Diagram:



* Sequential Circuit Design

State Diagram:

1110

1101

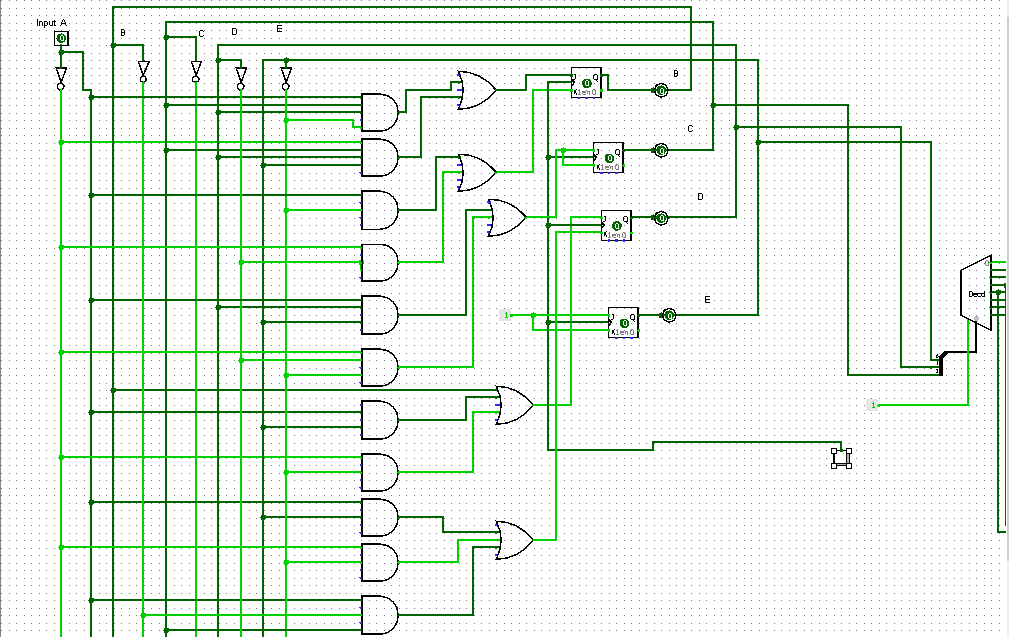
State Assignment:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| State | Binary Value Assignment | | | |
| C | 0 | 0 | 0 | 0 |
| S | 0 | 0 | 0 | 1 |
| E | 0 | 0 | 1 | 0 |
| 2 | 0 | 0 | 1 | 1 |
| 3 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| - | 0 | 1 | 1 | 0 |
| 1’ | 1 | 1 | 0 | 1 |
| -‘ | 1 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |

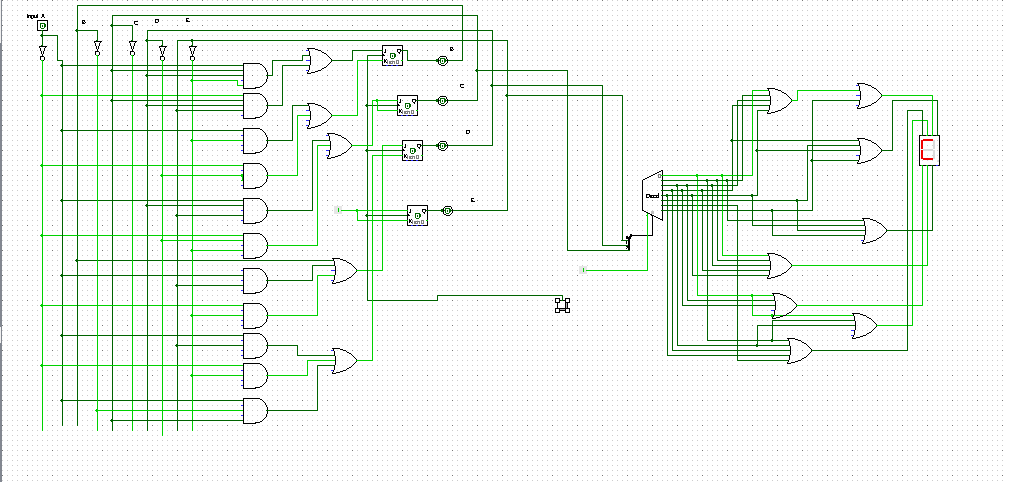
Truth Table

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| # | **Input** | **Present State** | | | | **Next State** | | | | **FF input Equations** | | | | | | | |
|  | **A** | **Bt** | **Ct** | **Dt** | **Et** | **Bt** | **Ct** | **Dt** | **Et** | **Jb** | **Kb** | **Jc** | **Kc** | **Jd** | **Kd** | **Je** | **Ke** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | X | 1 | X | 1 | X | 1 | X |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | X | 0 | X | 0 | X | X | 1 |
| 2 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | X | 0 | X | X | 1 | 1 | X |
| 3 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | X | 0 | X | X | 0 | X | 1 |
| 4 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | X | X | 1 | 1 | X | 1 | X |
| 5 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | X | X | 0 | 0 | X | X | 1 |
| 6 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | X | X | 0 | X | 1 | 1 | X |
| 7 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | X | X | 0 | X | 0 | X | 1 |
| 8 | 0 | 1 | 0 | 0 | 0 | X | x | x | x | X | X | X | X | X | X | X | X |
| 9 | 0 | 1 | 0 | 0 | 1 | x | x | x | X | X | X | X | X | X | X | X | X |
| 10 | 0 | 1 | 0 | 1 | 0 | X | x | x | x | X | X | X | X | X | X | X | X |
| 11 | 0 | 1 | 0 | 1 | 1 | x | x | x | X | X | X | X | X | X | X | X | X |
| 12 | 0 | 1 | 1 | 0 | 0 | X | x | x | x | X | X | X | X | X | X | X | X |
| 13 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | X | 1 | X | 0 | 1 | X | X | 1 |
| 14 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | X | 0 | X | 0 | X | 1 | 1 | X |
| 15 | 0 | 1 | 1 | 1 | 1 | x | x | x | X | X | X | X | X | X | X | X | X |
| 16 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | X | 0 | X | 0 | X | 1 | X |
| 17 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | X | 0 | X | 1 | X | X | 1 |
| 18 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | X | 0 | X | X | 0 | 1 | X |
| 19 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | X | 1 | X | X | 1 | X | 1 |
| 20 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | X | X | 0 | 0 | X | 1 | X |
| 21 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | X | X | 0 | 1 | X | X | 1 |
| 22 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | X | X | 0 | X | 1 | 1 | X |
| 23 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | X | X | 1 | X | 1 | X | 1 |
| 24 | 1 | 1 | 0 | 0 | 0 | X | x | x | x | X | X | X | X | X | X | X | X |
| 25 | 1 | 1 | 0 | 0 | 1 | x | x | x | X | X | X | X | X | X | X | X | X |
| 26 | 1 | 1 | 0 | 1 | 0 | X | x | x | x | X | X | X | X | X | X | X | X |
| 27 | 1 | 1 | 0 | 1 | 1 | x | x | x | X | X | X | X | X | X | X | X | X |
| 28 | 1 | 1 | 1 | 0 | 0 | X | x | x | x | X | X | X | X | X | X | X | X |
| 29 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | X | 0 | X | 0 | 1 | X | X | 1 |
| 30 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | X | 1 | X | 0 | X | 0 | 1 | X |
| 31 | 1 | 1 | 1 | 1 | 1 | x | x | x | x | X | X | X | X | X | X | X | X |

Circuit Diagram:



Logic Diagram:



Conclusion:

* While doing the project, the most common problem that we faced was the IC issue (faulty IC),hence we came to the conclusion that each IC after buying must be checked pin by pin.
* Some wires are more firmly attached to the breadboard than some other type of wires and a loose connection of wires can cause a mess out of nowhere. Hence, while choosing the wires to use, the best kind have to be considered.
* In sequential phase when we deal with flip-flops and timer circuit, special care has to be taken about the positive and negative edge trigger behavior of flip-flop. Otherwise, the output sequence will come as irregular than expected.
* While placing the connections between ICs , an erroneous idea of pin diagram can ruin the whole setup hence every pin diagram must be followed correctly.
* A must look up is to keep alert about active-high and active-low devices because a reciprocal connection of Vcc and GND may burn out any equipment.
* In our project, we have faced several unexpected problems in sequential phase, we never obtained the actual forward sequence. It had to be “C S E 2 3 1 – 1 -7” while we got “ C**7**S**7**E**7**2**7**3**7**1**7**-**7**1**7**-**7**7**7**”, we got 7 after each string . The simulation was working file while the placement on actual breadboard never worked out properly.